A Compact, Monolithic Microwave Demodulator-Modulator for 64-QAM Digital Radio Links

Isabelle Telliez, Anne-Marie Couturier, Christian Rumelhard, Christophe Versnaeyen, Philippe Champion, and Didier Fayol

***Abstract*—The design, fabrication and performances of a monolithic microwave direct modulation modulator-demodulator are presented. The subsystem is designed to work in a 64-QAM digital radio link. At this level of modulation, it is necessary to have some possibilities of phase and amplitude trimming by external voltages to achieve sufficient accuracy. The circuit includes elementary functions such as quadrature and in-phase splitters, two balanced mixers, a quadrature phase comparator, and circuits giving the possibility to adjust phases and amplitudes for 64 QAM and higher level modulation. The design is such that the same chip can be used either as a direct demodulator or as a modulator. This complex circuit of small dimensions (2.7 mm×3.65 mm) exhibits good demodulation and modulation performances. These overall performances of this monolithic circuit are achieved without degrading the dc yield.**

I. Introduction

THE USE of monolithic circuits is expanding in telecommunication equipments and the different circuits of receivers, or of transmitters, for satellite and digital microwave radio communications have been realized [1], [2]. However, for terrestrial telecommunications, the trend is to increase the spectral efficiency or the transmission capacity, and this is obtained by using sophisticated amplitude and phase modulation techniques (QPSK, 16, 64, or 256 QAM). Moreover, the conventional heterodyne solution for M-QAM demodulation is being replaced by direct (or homodyne) demodulation [3] which gives the advantage of the suppression of the IF circuits (lower costs, system simplification, reduced assembly). One of the most complex component to realize in a direct demodulation receiver is the demodulator. The first realizations of such circuits were in hybrid technology [4], [5].

For these complex circuits, the monolithic technology offers many advantages like the possibility of symmetrical design, the low spreads of the different components on a same chip. Besides, this technology allows a broad-band design, so that the same circuits can be used for many channels. With this technology, a complex circuit can be designed at affordable costs and with a reduction of size. An example of a monolithic homodyne phase detector working in S and L band was given in [6] and QPSK modulators working either in L or in X band were shown in [7] and [8]. But these circuits work only in four phase states and use an active circuit design which results in a high power consumption. A first realization of a low consumption demodulator realized with four MMIC chips has been reported [10]. The demodulator consisted of passive quadrature and in-phase couplers and of two balanced mixers [9].

But after the measurements with a 16 QAM modulation, it appeared that for a 64 QAM modulation it was necessary to add a possibility of adjusting the phase in the quadrature coupler and in the balanced mixers. A phase comparator was also necessary to test separately the exact quadrature in LO coupler. To have a low power consumption, the demodulator was realized with passive components and the mixer was designed with Schottky diodes. Thus, it has been possible to design a totally reciprocal demodulator which can also be used as a modulator. This avoids a special design for the modulator and decreases the cost of the set of monolithic chips for the total transmitter-receiver equipment (Fig. 1).

After a presentation of the diagram of the modulator-demodulator, the design of each circuit will be described: the quadrature and in-phase splitters, the phase and amplitude trimming circuits, the balanced mixers and the phase comparator. Then, the performances of the complete single chip used as a modulator and as a demodulator will be shown.

II. Circuit Design

The use of high level M-QAM modulation makes microwave links more sensitive to manufacturing spreads, and phase errors. In particular, the quadrature phase error in the demodulator increases the BER (bit error ratio) of a radio-link.

The phases and amplitudes in the quadrature LO signal splitter, and in the balanced mixers must be adjustable to

Manuscript received April 12, 1991; revised September 3, 1991.
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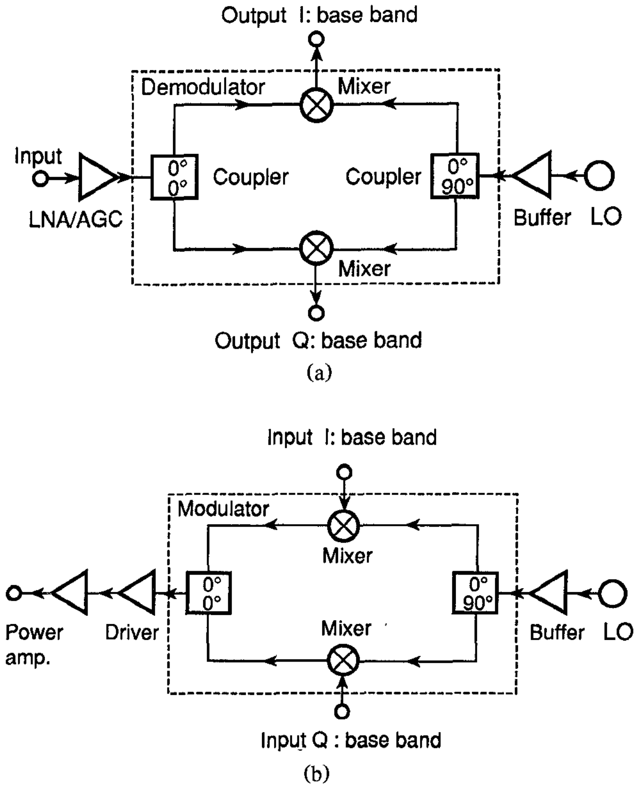

Fig. 1. Block diagrams. (a) Direct demodulation receiver. (b) Direct modulation transmitter.

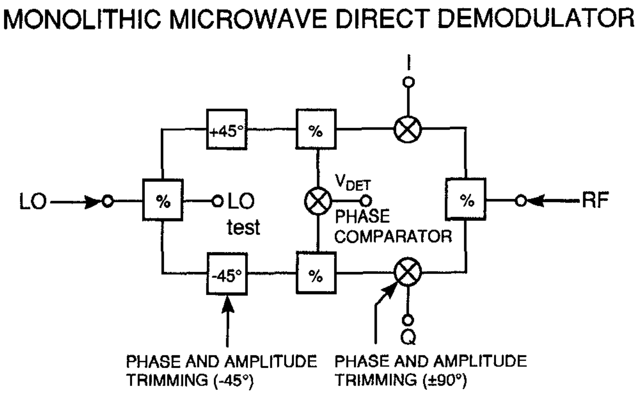

Fig. 2. Block diagram of the multi-level modulation demodulator.

meet the system requirements, and to compensate for functional imperfections due to manufacturing tolerances or thermal drifts. These reflexions have led to the block diagram of the multi-level modulation demodulator-modulator (Fig. 2). A phase comparator was added in order to control separately and automatically the quadrature phase adjustment in the LO splitter. The subsystem includes two power splitters, a LO level test, a quadrature phase comparator, adjustable $\pm 45°$ and $\pm 90°$ phase-shift sections, and two single balanced mixers.

A. RF and LO Splitters

RF and LO signals are applied through 2 way- and 3 way-lumped element Wilkinson couplers respectively. Two

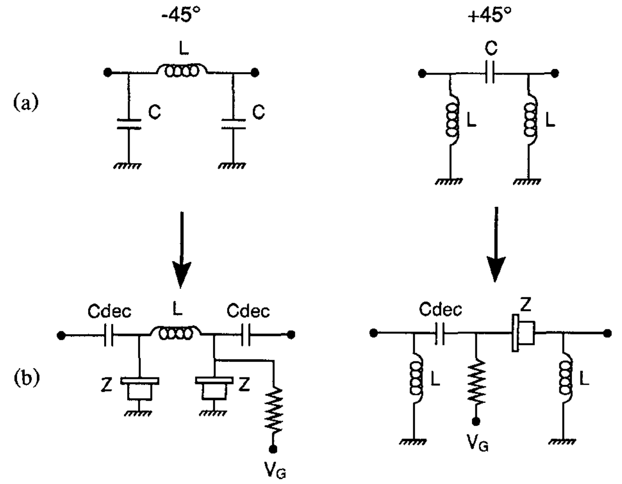

Fig. 3. Electrical schematic of $\pm 45°$ phase-shift sections. (a) Fixed lumped element version. (b) Adjustable version.

45° phase-shift sections were cascaded to broaden the pass-band.

The choice of a passive solution for the RF coupler provides reciprocal operation so that the circuit can be used either as a modulator or a demodulator.

B. Adjustable Phase-Shift Sections

The quadrature phase is realized with $\pm 45°$ lumped element phase-shift sections. To achieve a simultaneous phase and amplitude adjustment, these high-pass and low-pass "pi" networks use the variable capacitance of MESFET's connected as varactors, instead of an overlay capacitor (Fig. 3). The phase and amplitude are trimmed with the gate bias varying from 0 V to pinch-off voltage: measurements of these phase-shift sections are presented in Fig. 4.

C. Quadrature Phase Comparator

The configuration selected uses two diodes, and the two signals to be compared are applied to the two diodes, respectively in phase and out of phase (see Fig. 5). With this configuration, a dc voltage directly proportional to $\cos\varphi$ (where φ is the phase-shift between the two input signals to compare) is obtained, without an offset voltage which is the case for a single diode topology.

The input signals can be expressed as

$$e_1 = E_1 \cos(\omega t) \tag{1}$$

$$e_2 = E_2 \cos(\omega t + \varphi). \tag{2}$$

Vd_1, Vd_2 are the detected voltages by the matched pair of diodes $D1$ and $D2$, respectively:

$$Vd_1 = k\left(E_1^2 + E_2^2 + 2E_1E_2\cos\varphi\right) \tag{3}$$

$$Vd_2 = k\left(E_1^2 + E_2^2 - 2E_1E_2\cos\varphi\right). \tag{4}$$

The total detected voltage is then

$$Vd = Vd_1 - Vd_2. \tag{5}$$

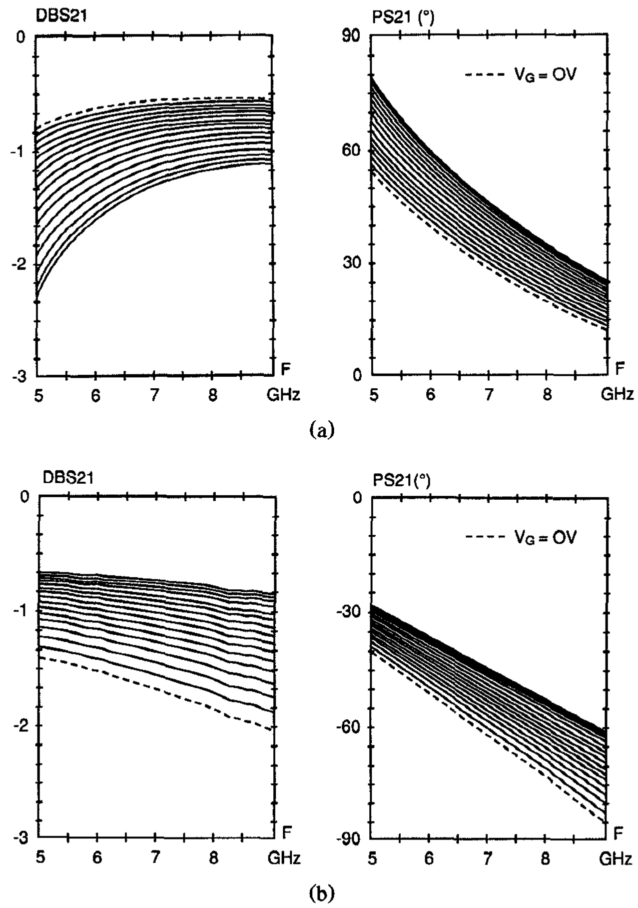

Fig. 4. Transmission measurements of the adjustable 45° phase-shift sections, when the gate bias varies from 0 V to pinch-off voltage. (a) +45° phase-shift section. (b) −45° phase-shift section.

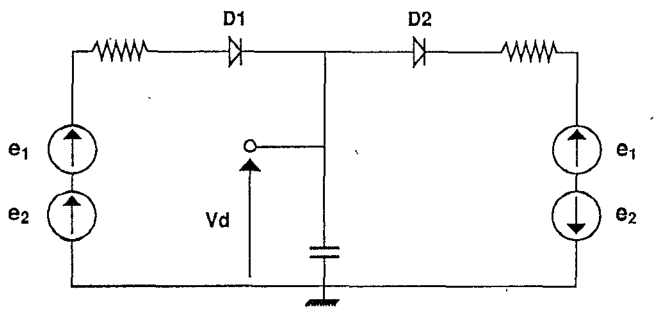

Fig. 5. Basic topology for the quadrature phase comparator.

Thus,

$$Vd = 4kE_1E_2\cos\varphi. \tag{6}$$

However, if the input signals are not perfectly symmetric between the two diodes, or if the pair of diodes are not well matched, an additional phase-shift φ_o appears, and the detected dc voltage becomes

$$Vd = 4kE_1E_2\cos(\varphi + \varphi_o). \tag{7}$$

As in our application, φ is in fact equal to $(\Pi/2 + \Delta\phi)$, the detected voltage exhibits different values, when the sign of $(\Delta\phi)$ changes. This enables an automatic loop to control the quadrature angle.

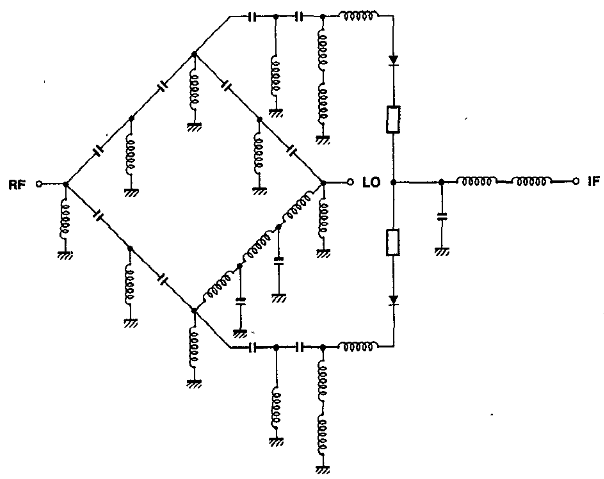

Fig. 6. Schematic of the quadrature phase comparator.

Another point of view is to consider this circuit as a single balanced mixer. So, the design of the quadrature phase comparator is equivalent to the design of a balanced mixer where the IF is equal to zero [9]. Designing a mixer consists of solving two problems: the design of the balun, and the choice of the nonlinear element. A classical way to realize the balun is the ring hybrid (rat-race) that splits the microwave input signals (RF, LO) between the two diodes, in phase and out of phase respectively. This kind of hybrid is realized with quarter-wavelength transmission lines of characteristic impedance $Z\sqrt{2}$. A monolithic approach of the rat-race is to replace the quarter-wavelength by their lumped element low- and high-pass equivalents. Again, 45° phase-shift sections were actually used to broaden the pass-band (Fig. 6). The amplitude and phase imbalances between the diode terminal voltages are less than ± 0.5 dB and $\pm 2.5°$, respectively, for both signals over the frequency range 5.9 GHz–8.5 GHz. To the output ports of the lumped element ring, two identical RF matching networks are added. Each of them comprises spiral inductors in shunt to ground, that provides a dc and an IF ground-return. A low-pass filter on the output port rejects the RF (and LO) signals, and improves RF to IF isolations.

D. Mixers

Direct demodulation enables the suppression of the intermediate frequency, and the output frequency called IF frequency is in fact the baseband, i.e., a few kHz to 300 MHz. This implies that RF and LO signals are very close.

As for the quadrature phase comparator, Schottky diodes were selected as the nonlinear element for the mixers due to the following advantages: first, they do not need dc bias circuitry, which implies zero dc power consumption for the whole demodulator; second, the low number of active components leads to a good yield and smaller electrical spreads; third, the diodes exhibit a lower noise figure than single-gate and dual-gate MESFET's below 10 MHz ($1/f$ noise).

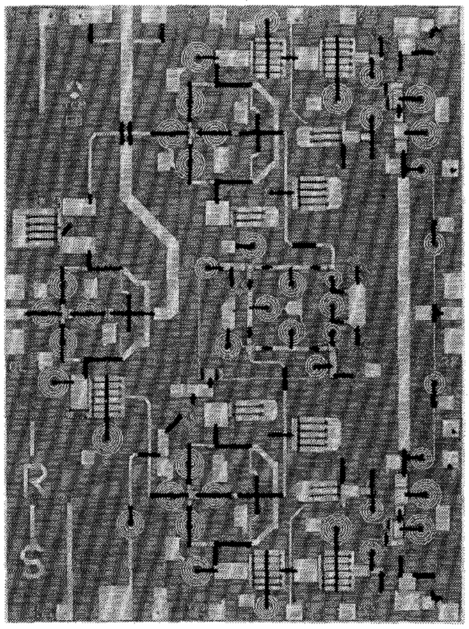

Fig. 7. Photograph of the demodulator-modulator.

Since the RF and LO signals closely share the same band (5.9 GHz–8.5 GHz), a filter could not be used to suppress LO signal, and the mixer had to be a 180° balanced configuration, hence providing good LO to RF isolation. The phase comparator of the preceding section could be used as a balanced mixer. But this configuration would involve a supplementary phase trimming in the RF way, to preserve the symmetry of the ring.

The configuration of mixer which has been chosen is the following. The LO signal is fed to the $\pm 90°$ phase-shifters from two outputs of a lumped element 3 way-Wilkinson, the third path is an input of the quadrature phase comparator. The $\pm 90°$ phase-shifters are achieved by cascading $\pm 45°$ adjustable phase-shift sections (see Section II-B).

Between the diodes and the adjustable $\pm 90°$ phase shifters, identical matching networks are added. A spiral inductor in shunt to ground included in these networks provides a dc and IF ground-return. At the middle node between the diodes, a lumped element diplexer is used to apply and extract the RF and baseband signals. The diplexer consists of a five element Chebyshev high-pass filter and a four element butterworth low-pass filter. These choices give the best trade-off between the losses in pass-band and the rejection in the stop-band. The high-pass filter is then connected to the RF splitter.

III. Circuit Layout and Fabrication Process

The layout was carried out with special care to preserve the symmetry of the sub-block functions and thus to achieve amplitude and phase balances. The circuit, of small dimensions 2.7×3.65 mm^2, is composed of 68 inductors, 68 capacitors, 46 via-holes, 121 air-bridges, six diodes of 64 μm total gate width (Fig. 7). The total gate width for the MESFET's is 6.75 mm, but these MESFET's work with a zero drain voltage.

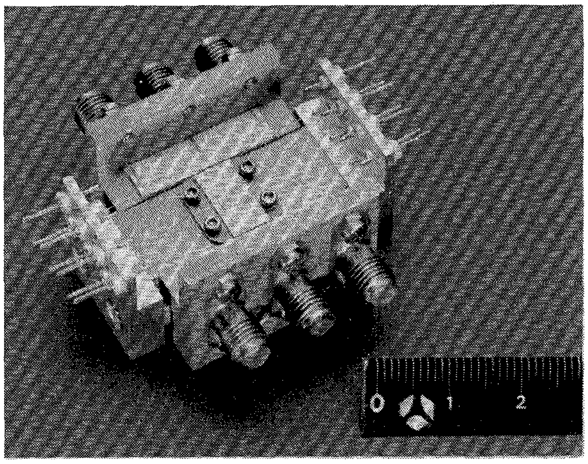

Fig. 8. Photograph of the circuit in its test fixture.

The circuits have been fabricated at Thomson Composants Microondes Foundry with its standard LN05 process. The main LN05 process features are ion implanted active layers, TiPtAu 0.5 μm gate length MESFET's and diodes, implanted and metallic resistors, Si_3N_4 overlay capacitors, spiral inductors, air bridges and via-holes through 100 μm thick wafer.

Automatic dc wafer testing was conducted upon all circuits at the end of the fabrication process, and despite the circuit complexity, the dc yield was better than 70% on eight good wafers.

IV. Performances

The photograph of the chip mounted in its test fixture is presented in Fig. 8.

A direct demodulator has to be characterized as a down-converter to measure its conversion loss and its linearity, and as a demodulator to measure the accuracy of the quadrature, the LO rejection, the eye closures. The subsystem was characterized as a down-converter (and an up-converter) over the whole range of frequencies. Then it has been measured in a digital radio-link over the 6.4 GHz–7.1 GHz range as a 64 QAM and a 16 QAM demodulator. It was also measured as a 16 QAM modulator.

A. Measurements as a Frequency Converter

The circuit has been measured over 5.9 GHz–8.5 GHz range for the LO and RF signals, and from 50 MHz to 350 MHz for the IF. The conversion losses are 11 ± 1 dB over the frequency bands as a double up- and down-converter. The LO power applied is 20 dBm. An important parameter to check out for a demodulator is its linearity, which consists of measuring the 1 dB compression point. The 1 dB compression point is found out for an input RF power of 5 dBm as a down-converter, and for an IF input power higher than 5 dBm as an up-converter. The LO-RF isolations are higher than 35 dB in both cases of operation.

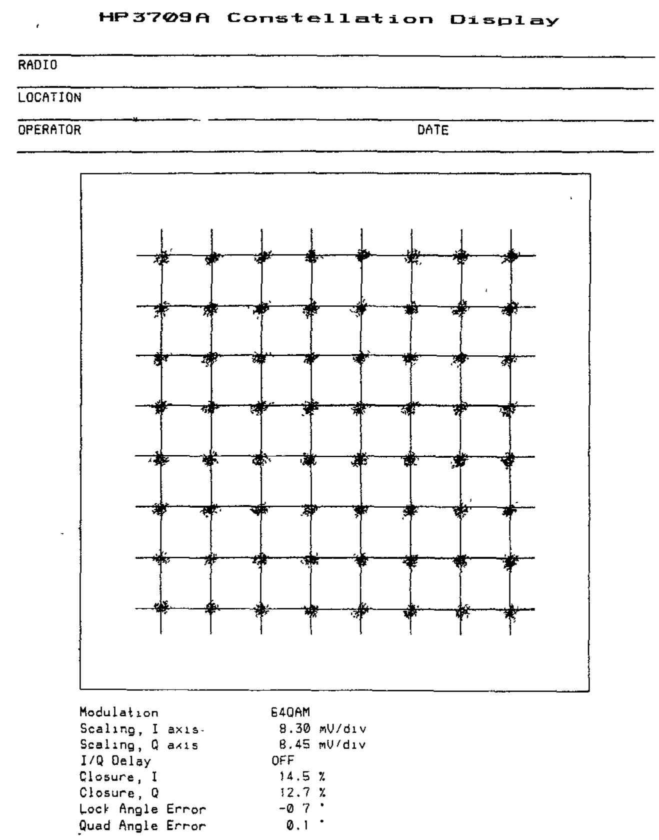

Fig. 9. 64 QAM constellation at 6.8 GHz; the circuit is operating as demodulator.

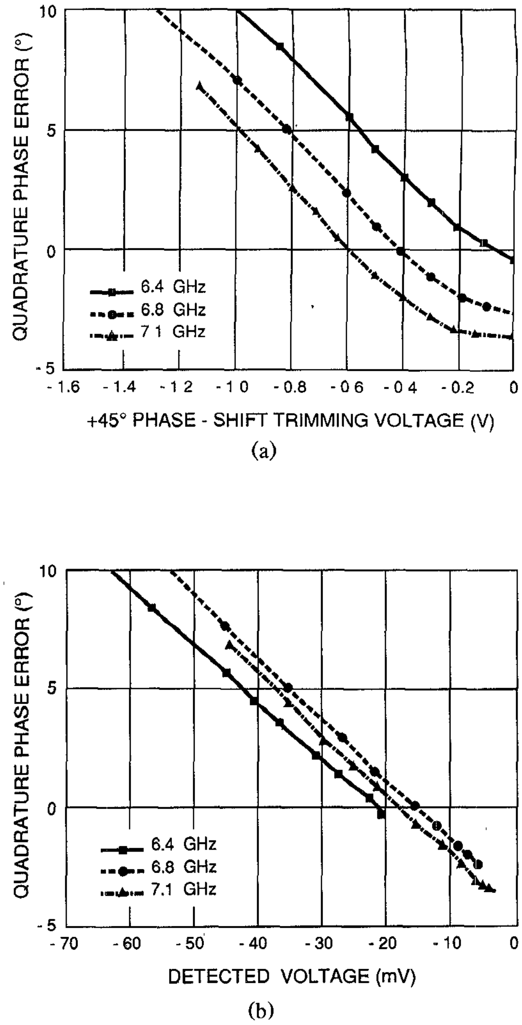

Fig. 10. 64 QAM demodulation performances as a function of frequency and of quadrature trimming voltages. (a) Variation of quadrature phase error with quadrature phase trimming voltage (+45° phase-shift section here). (b) Variation of quadrature phase error versus detected voltage of the phase comparator, recorded during the constellation measurements of (a).

B. Performances as a Demodulator

A way to evaluate the modulator-demodulator performance is to display the constellation diagram, which is the representation in the complex plane of all the amplitude and phase states presented by the output signals (I and Q). One important parameter extracted from this constellation display is the quadrature phase error (quad angle error): this angle measures the error of quadrature between the two signals I and Q (ideally in quadrature). This error should remain as little as possible over the whole band, otherwise errors would appear in the signal transmission. The constellation diagrams also give the eye closures on I and Q paths.

An original bench was developed at Alcatel–Telspace for the characterization of the direct demodulator [11]. The difficulty in characterizing such a device is to generate to the direct demodulator a perfect microwave modulated signal. An heterodyne solution is used: a signal is first modulated at 140 MHz, and then up-converted at the desired microwave frequency. A data generator (HP3762A) generates pseudo-random binary sequences to a vector signal generator (HP8780A) which is considered as an ideal M-QAM modulator. The output signal is M-QAM modulated at 140 MHz. A microwave signal generator provides the carrier frequency "f" to two mixers. One of these mixers up-converts the modulated signal (at $f+140$ MHz), the other one provides after some filtering and amplification the LO signal to be applied to the demodulator under test. At the outputs of the demodulator under test the baseband signals I and Q are fed to the constellation analyzer (HP8981 for example). A frequency counter measures the frequency "f", and a spectrum analyzer displays the spectrum to demodulate. To evaluate the performance of the demodulator at the frequency "fa", f must be equal to ($fa-140$ MHz), and the filter must be tuned at fa. To get performances at "M" points of frequency, "M" tuned filters must be available.

Fig. 9 shows a typical 64 QAM constellation diagram obtained at 6.8 GHz, for a data transmission rate of 140 Mbit/s. At each frequency, with adequate trimming, the quadrature phase error measured is lower than 0.5°. The quadrature phase error variation is lower than $\pm 1.5°$ all over the 6.4 GHz–7.1 GHz range for a quadrature phase adjusted at 6.8 GHz.

The quadrature phase error varies linearly with each trimming voltage, when the other trimming voltages are fixed (Fig. 10). These linear variations of the quadrature

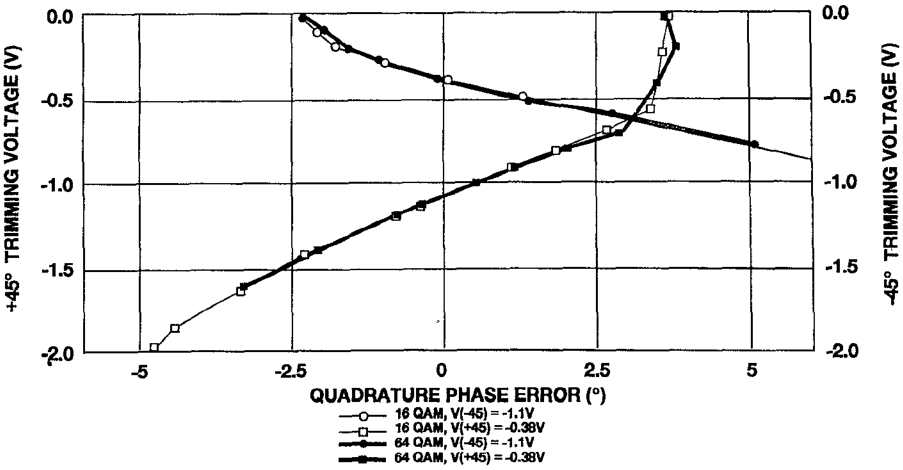

Fig. 11. Variations of the quadrature phase error with quadrature trimming voltages, for 16 QAM and 64 QAM modulations.

phase error allow simple control laws of the trimming voltages. These variations of the quadrature phase error with the quadrature trimming voltages are the same whatever the type of modulation is (16 QAM or 64 QAM, Fig. 11).

During these measurements, the linear response of dc voltage detected at the output of the phase comparator was recorded (Fig. 10). This linear response enables the design of a loop to lock onto the quadrature phase.

C. Performances as a Modulator

Another bench was developed to characterize the performance of a direct modulator [11]. In this case, the task is to compare a real microwave modulated signal to an ideal modulated signal. The solution adopted is to use a known direct demodulator (hence characterized with the previous bench), in order to demodulate the signal created by the direct modulator under test. Then the baseband signals (I and Q) generated by this assembly are compared to the "perfect" baseband signals applied to it, by means of a constellation analyzer. A microwave frequency generator provides a carrier "f" to the modulator under test and to an hybrid demodulator [4] already characterized with the previous bench (Section III-B). At the outputs of this demodulator, the baseband signals are displayed on a constellation analyzer. A frequency counter measures the frequency "f", and the spectrum analyzer displays the spectrum modulated. To evaluate the performance of the modulator at the frequency "fa", the frequency f must be made equal to fa.

A typical 16 QAM constellation diagram obtained with this monolithic modulator is shown in Fig. 12: the carrier frequency is 6.4 GHz, the data transmission rate is 140 Mbit/s. As seen before, the quadrature phase error varies linearly with each trimming voltage, when the other trimming voltages are fixed. The dc voltages recorded at the output of the phase comparator during these constellation measurements vary linearly.

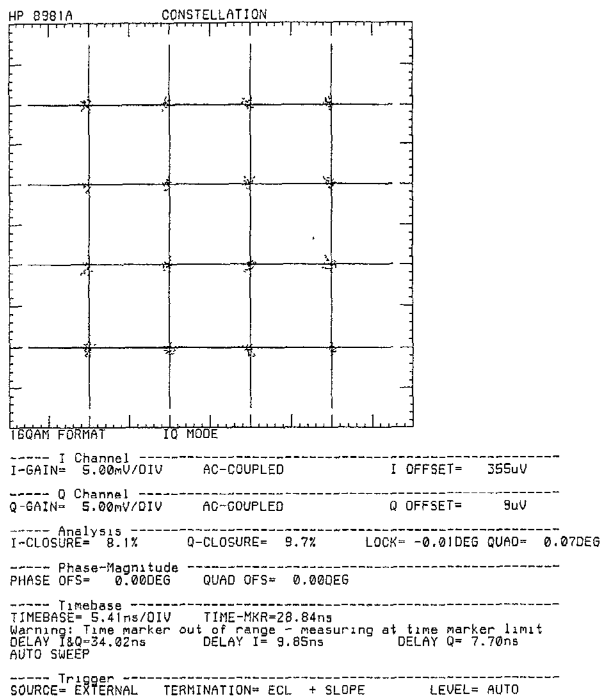

Fig. 12. 16 QAM constellation at 6.4 GHz, as a modulator.

V. Conclusion

A single chip monolithic 64 QAM demodulator-modulator with phase and amplitude trimming and with a quadrature phase test has been implemented. This circuit works in the 5.9 GHz–8.5 GHz range. The design of the different component circuits of the demodulator has been described: the quadrature phase comparator, the adjustable 45° phase-shift sections, the balanced mixers, the LO and RF couplers. As all these sub-blocks contain only passive elements and diodes, the whole circuit is reciprocal, and can be used as a demodulator or a modulator. This circuit was characterized as a modulator with 16 QAM pattern and as a demodulator with 16 QAM and 64 QAM modulations. The high performances achieved allow its integration into future ground radio-link equipments.

This design shows the ability offered by the monolithic technology to achieve high performance circuits with a high level of integration, low dc power supply and good yield. This achievement demonstrates the maturity of the present GaAs technology.

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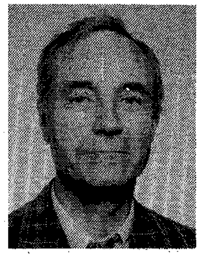
From 1985–1987, she worked at Thomson Composants Microondes towards the doctor degree, on large-signal FET modeling and power amplifier design.

She joined Thomson Composants Microondes in 1987, where she is involved in MMIC design, more particularly MMIC for direct demodulation receivers and high-efficiency power amplifiers. She is currently a MMIC project manager and design group leader for T/R modules.

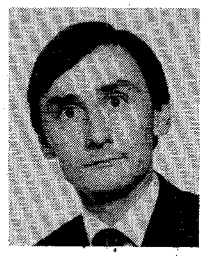
Anne-Marie Couturier received the DUT degree in electronics in 1985.

She then worked at Thomson Semiconducteurs (Tours, France), in the Application Laboratory for RF bipolar transistors. She joined Thomson Composants Microondes in 1986 (the Gallium Arsenide Foundry of Thomson group) where she has been involved in the design of wideband VCO's, doublers, couplers and MMIC's for direct demodulation receivers. She is currently developing a product family of switches.



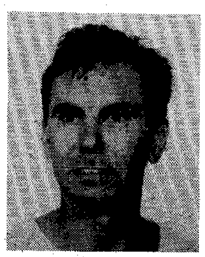
Christian Rumelhard qualified as Electrical Engineer, Conservatoire National des Arts et Métiers, Paris, in 1966 and received the Docteur Ingénieur degree from the University of Paris VI in 1977.

Until 1969, he worked at Thomson-Varian, on the development of microwave power tubes. From 1969 to 1977, he was involved in the design of hybrid microwave integrated circuits in the Microwave Microelectronic Department of Thomson-CSF. In 1975, he joined the Computer Science Division of the same company to develop computer aided design algorithms and numerical models for the simulation of microwave circuits and devices. In 1980, he was head of the Monolithic Microwave Integrated Circuit Laboratory of Central Research Laboratory of Thomson where he worked on the increasing of integration density of MESFET monolithic circuits and on TEGFET (HEMT) monolithic circuits. In 1985, he became manager of a MMIC design, models and measurement group at Thomson Composants Microondes. The result of this activity was the design and realization of about a hundred different monolithic circuits between 1 and 20 GHz. From the beginning of 1991, he has been Senior Scientist in the Electron Device Group of Central Research Laboratory, working mainly on the modeling and design of PM-HEMT and HBT monolithic circuits.



Christophe Versnaeyen was born in Armentieres, France in 1960. He received a third degree thesis on Heterojunction Field Effect Transistor, in 1985.

He joined Thomson Composants Microondes in 1986, where he was involved in MMIC design for T/R modules (phase-shifter and control circuits). Until 1991, he was a MMIC project manager and a MMIC design group leader. He is currently managing the integrated circuit test and measurement group.



Philippe Champion was born in St. Dizier, France in 1959. He received the DUT degree in electronics from the University of Troyes, France, in 1980, and studied the telecommunication systems in the University of Reims, France, in 1981.

From 1982 to 1989, he worked on microwave sub-assemblies for telecommunication systems in the microwave laboratory of Alcatel Telspace. In 1989, he joined the Monolithic Microwave Integrated Circuits Laboratory of Alcatel Telspace, where he has been dealing with MMIC packaging and characterization of direct modulator/demodulator and various microwave circuits for space diversity microwave combiner.

Didier Fayol was born in Pithiviers, France, in 1960. He received the DUT degree in electronics from the University of Ville d'Avray, France, in 1980, and the diploma of electrical engineering from E.N.S.E.A., Cergy, France, in 1988.

He joined the Microwave Laboratory of Alcatel Telspace in 1980, where he worked on microwave sub-assemblies for telecommunication systems, especially on finline mixers, dielectric resonator oscillators and direct hybrid modulator/demodulator. In 1989, he joined the Monolithic Microwave Integrated Circuits Laboratory of Alcatel Telspace, where he designed amplifiers, and was involved in the characterization of a microwave modulator/demodulator chip. Since 1990, he has been a system manager responsible for the microwave CAD softwares and hardwares used in Alcatel.